Patent claims

1. A method for fabricating an integrated pin diode (14), in particular a pin photodiode (14),

having the following steps executed without a restriction by the order specified:

production of a doped region (20) of one conduction type, which, in respect of a carrier substrate (12), is near the substrate,

production of a doped region (42) remote from the substrate, which is further away from the carrier substrate (12) than the region (20) near the substrate and is of a different conduction type than the conduction type of the region (20) near the substrate,

production of an intermediate region (30), which is arranged between the region (20) near the substrate and the region (42) remote from the substrate and is undoped or provided with a weak doping in comparison with the doping of the region (20) near the substrate and the doping of the region (42) remote from the substrate,

and production of at least one electrically conductive terminal region (32), which leads to the region (20) near the substrate, in a layer (55) containing the intermediate region (30).

2. The method as claimed in claim 1, wherein the terminal region (32) penetrates through the layer (55) from its interface remote from the substrate as far as its interface near the substrate.

3. The method as claimed in claim 1 or 2, comprising the steps of:

production of a doped decoupling region (22) at the same time as the production of the region (20) near the substrate,

and production of a circuit arrangement (10) carried by the carrier substrate and having at least two components (58, 60, 82), the decoupling region (22) preferably being arranged between one portion of the components (58, 60) and the carrier substrate (12) and not between the other portion of the components (82) and the carrier substrate (12).

4. The method as claimed in claim 3, comprising the step of:

production of an electrically conductive decoupling region terminal region (56) at the same time as the production of the terminal region (32) leading to the region (20) near the substrate.

5. The method as claimed in claim 4, wherein the decoupling region terminal region (56) and the decoupling region (22) form a shielding well which surrounds a region encompassed by the shielding well completely or, relative to the side areas and the base area of the encompassed region, by at least fifty percent or by at least seventy five percent.

6. The method as claimed in one of claims 3 to 5, wherein, in the layer (55) in which the region (20) near the substrate and the decoupling region (22) are arranged, regions outside said regions (20, 22) are provided with a doping of a different conduction type, an oxide (130) covering the region (20) near the substrate and the decoupling region (22) preferably serving for masking implantation (140),

or wherein, in the layer (55) in which the region (20)

near the substrate and the decoupling region (22) are arranged, regions outside said regions (20) are undoped or selectively doped.

7. The method as claimed in one of the preceding claims, wherein the terminal region (32, 56) is produced with the fabrication of a trench which preferably has a depth that is at least twice its width,

or wherein the terminal region (32, 56) is fabricated with the aid of a diffusion process in which dopants diffuse from a region remote from the substrate as far as the layer (20) near the substrate,

and/or wherein the terminal region (32, 56) is produced by an implantation method, preferably by a high-energy implantation method.

8. The method as claimed in one of the preceding claims, wherein the layer (55) containing the intermediate region (30) is produced by an epitaxy method,

and/or wherein a base material for an embedding region (52, 54), which serves for embedding components (58, 60, 82) of an integrated circuit arrangement (10), is produced simultaneously during the epitaxy method.

9. The method as claimed in claim 8, wherein an epitaxy method for producing an epitaxial layer is conducted in at least two stages,

the epitaxial growth being interrupted,

the interruption being followed by the execution of at least one other process, preferably a doping process for fabricating a doping which differs from a doping of

the epitaxial layer,

and the growth of the epitaxial layer being continued after the execution of the other process.

10. The method as claimed in one of the preceding claims, wherein the terminal region (32) leading to the region (20) near the substrate laterally encompasses the intermediate region (30), preferably completely.

11. The method as claimed in one of the preceding claims, wherein the layer (55) containing the intermediate region (30) is a semiconductor layer which preferably contains regions with different conduction types.

12. The method as claimed in one of the preceding claims, wherein the decoupling region (22) adjoins material (12, 52, 54) with a different conduction type or is surrounded by material with a different conduction type, preferably on all sides apart from one or a plurality of decoupling region terminal regions (56).

13. An integrated circuit arrangement (10) having a pin diode (14), in particular having a pin photodiode (14),

having a carrier substrate (12), which carries a region sequence of a pin diode (14),

having a doped region (20) of one conduction type, which is contained in the region sequence and is near the substrate,

having a doped region (42) remote from the substrate, which is contained in the region sequence and is of a different conduction type than the conduction type of

the region (20) near the substrate,

having an intermediate region (30) which is arranged between the region (20) near the substrate and the region (42) remote from the substrate and is undoped or provided with a weak doping in comparison with the doping of the region (20) near the substrate and the doping of the region (42) remote from the substrate,

and having an electrically conductive terminal region (32), which leads to the region (20) near the substrate and is arranged in a layer (55) containing the intermediate layer (30).

14. The circuit arrangement (10) as claimed in claim 13, wherein the terminal region (32) penetrates through the layer (55) from its interface remote from the substrate as far as its interface near the substrate.

15. The circuit arrangement (10) as claimed in claim 13 or 14, comprising a circuit arrangement (10) which is carried by the carrier substrate (12) and contains at least two electronic components (58, 60, 82),

and a doped decoupling region (22) arranged between the one component (58) and the carrier substrate (12) and of the same conduction type as the region (20) near the substrate and/or of the same dopant concentration as the region (20) near the substrate and/or arranged in one plane with the region (20) near the substrate.

16. The circuit arrangement (10) as claimed in claim 15, comprising an electrically conductive decoupling region terminal region (56), which leads to the decoupling region (22) and/or which has the same material composition as the terminal region (32)

leading to the region (20) near the substrate.

17. The circuit arrangement (10) as claimed in one of claims 13 to 16, wherein the circuit arrangement (10) has been fabricated by a method as claimed in one of claims 1 to 12.